IN THE CLAIMS

Please amend claim 38 as follows:

1. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which wiring grooves are formed.

2. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and the specific dielectric constant of the first dielectric layer is relatively smaller than the specific dielectric constant of the second dielectric layer.

3. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and the hole diameter of the via hole is about 0.5 μm or less.

4. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and a stopper dielectric film of a relatively

thin film thickness is formed between the first dielectric layer and the second dielectric layer.

5. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and a main conductive layer constituting the wirings is made of copper.

6. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of the first dielectric layer in which the via holes are formed is less than 60 GPa and the Young's modulus of the second dielectric layer in which the wiring grooves are formed is 60 GPa or more.

7. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of SiOF and the second dielectric layer in which the wiring grooves are formed is constituted of SiO_2.

8. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of SiOF and the second dielectric layer in which the wiring grooves are formed is constituted of SiO_2, and the hole diameter of the via hole is about 0.5 μm or less.

9. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of SiOF and the second dielectric layer in which the wiring grooves are formed is constituted of SiO_2, and a stopper dielectric film of relatively thin film thickness comprising SiN or SiC is formed between the first dielectric layer and the second dielectric layer.

10. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of the first dielectric layer in which the via holes are formed is less than 30 GPa, and the Young's modulus of the second dielectric layer in which the wiring grooves are formed is 30 GPa or more.

11. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the second dielectric layer in which the wiring grooves are formed is constituted of SiOF or SiO_2.

12. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the second dielectric layer in which the wiring grooves are formed is constituted of SiOF or SiO_2, and the hole diameter of the via hole is about 0.2 μm or less.

13. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the second dielectric layer in which the wiring grooves are formed is constituted of SiOF or SiO_2, and a stopper dielectric film of relatively thin film thickness comprising SiN or SiC is formed between the first dielectric layer and the second dielectric layer.

14. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of the first dielectric layer in which the via holes are formed is less than 6 GPa and the Young's modulus of the second dielectric layer in which the wiring grooves are formed is 6 GPa or more.

15. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of a porous HSQ type material and the second dielectric layer in which the wiring grooves are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of an SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material.

16. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of a porous HSQ type material and the second dielectric layer in which the wiring grooves are formed is constituted of an SiOC type material, CF type material,

HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of an SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the hole diameter of the via hole is about 0.13 μm or less.

17. (Withdrawn) A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of a porous HSQ type material and the second dielectric layer in which the wiring grooves are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of an SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and a stopper dielectric film of a relatively thin film thickness comprising SiO_2 is formed between the first dielectric layer and the second dielectric layer.

18-27. (Canceled)

28. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 30 GPa and a second dielectric layer having a Young's modulus of 30 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

29. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via

holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 30 GPa and a second dielectric layer having a Young's modulus of 30 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the first dielectric layer is formed by a CVD method or coating method and the second dielectric layer are formed by a CVD method

30. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material and a second dielectric layer is constituted of SiOF or SiO_2 successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

31. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material and a second dielectric layer is constituted of SiOF or SiO_2 successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the hole diameter of the via hole is about 0.2 μm or less.

32. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material and a second dielectric layer is constituted of SiOF or SiO_2 successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a stopper dielectric film comprising SiN or SiC of a relatively thin film thickness is formed to an upper layer of the first dielectric layer in the step (a) and wiring grooves are formed at a predetermined region in the second dielectric layer and the stopper dielectric film in the step (b).

33. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 6 GPa and a second dielectric layer having a Young's modulus of 6 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

34. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 6 GPa and a second dielectric layer having a Young's modulus of 6 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the first dielectric layer is formed by a coating method and the second dielectric layer are formed by a CVD method or coating method.

35. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of a porous HSQ type material and a second dielectric layer constituted of an SiOC material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material BCB type material or PAE type material successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

36. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via

holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of a porous HSQ type material and a second dielectric layer constituted of an SiOC material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material BCB type material or PAE type material successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the hole diameter of the via hole is about 0.13 μm or less.

37. (Withdrawn) A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of a porous HSQ type material and a second dielectric layer constituted of an SiOC material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material BCB type material or PAE type material successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a stopper dielectric film comprising SiO_2 of relatively thin film thickness is formed to an upper layer of the first dielectric layer in the step (a) and wiring grooves are formed at predetermined regions in the second dielectric layer and the stopper dielectric film in the step (b).

38. (Currently amended) A method of fabricating a semiconductor integrated circuit device, comprising:

(a) forming a lower layer dielectric film including a first silicon oxide film containing fluorine over a major surface of a wafer;

(b) forming an upper layer dielectric film including a second silicon oxide film substantially without fluorine as compared with the first silicon oxide film over the first silicon oxide film, the upper and lower layer dielectric films constituting an inter-layer dielectric film having an inter-wiring layer portion embedded in the upper layer dielectric film and an inter-via layer portion embedded in the lower layer dielectric film respectively;

(c) forming via holes through said upper dielectric film and said lower dielectric film and then forming wiring grooves in the upper dielectric film, wherein at least one of said wiring grooves includes one of said via holes in a groove pattern, said at least one of the wiring grooves and said one of said via holes are connected therethrough, and said at least one of the wiring grooves has an area larger than an area of said one of said via holes in plan view;

(d) forming a barrier metal along said wiring grooves and via holes and then filling said at least one of the wiring grooves and [[the]] said one of said via holes with copper so as to integrally form an embedded wiring and a copper plug electrically connecting the embedded wiring to a lower wiring or electrode,

wherein a Young's modulus of the lower dielectric film ~~as a whole~~ is smaller than that of the upper dielectric film.

39. (Previously presented) A method of fabricating a semiconductor integrated circuit device according to claim 38, wherein a stopper dielectric film is formed between the inter-wiring layer portion and the inter-via layer portion.

40. (Previously presented) A method of fabricating a semiconductor integrated circuit device according to claim 39, wherein the stopper film is a SiC film.

41. (Previously presented) A method of fabricating a semiconductor integrated circuit device according to claim 39, wherein the stopper film is a SiN film.

42. (Previously presented) A method of fabricating a semiconductor integrated circuit device according to claim 38, wherein a stopper dielectric film is not formed between the inter-wiring layer portion and the inter-via layer portion.